## REMARKS

This paper is being provided in response to the October 21, 2002 Final Office Action for the above-referenced application. In this response, Applicant has amended Claims 1, 2, 15, 16, and 18 in order to clarify that which Applicant deems to be the invention. Applicant respectfully submits that the modifications to the Claims are supported by the originally-filed application.

Applicant thanks the Examiner for allowing Claims 7-8 and 13-14.

The rejection of Claims 1-5, 9-11, and 15-18 under 35 U.S.C. 102(b) as being anticipated by Tanaka et al. (U.S. Patent No. 4,970,694) is hereby traversed and reconsideration thereof is respectfully requested in view of amendments to the claims contained herein. Applicant respectfully submits that Claims 1-5, 9-11, and 15-17, as amended herein, are patentable over the cited reference.

Claim 1, as amended herein, recites a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level. An inverter chain contains not less than one inverter. A metal-oxide-semiconductor capacitor, known as a MOS capacitor, has a single transistor per stage of the inverter chain connected to an output section of the inverter and, when a logic signal having a targeted logic level is input, changes from an off-state to an on-state during a transition period of a signal that appears in the output section of the inverter. Each stage is tied alternately to one of a power voltage source and a ground voltage source. The MOS

capacitor is represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage. Claims 3-5 depend from Claim 1.

Claim 2, as amended herein, recites a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level. An inverter chain contains not less than one inverter. A metal-oxide-semiconductor capacitor, known as a MOS capacitor, has a single transistor per stage of the inverter chain connected to an output section of the inverter and exhibits changes in its capacitance to correspond with changes in output resistance of the inverter in relation to a source voltage. Each stage is tied alternately to one of a power voltage source and a ground voltage source. The MOS capacitor is represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage. Claims 9-11 depend from Claim 2.

Claim 15, as amended herein, recites a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level. An inverter chain contains not less than four inverters. A p-channel metal-oxide-semiconductor transistor and an n-channel metal-oxide-semiconductor transistor, known as MOS transistors, comprise each of the at least four inverters, wherein a gate threshold voltage of each gate is shifted in mutually opposing directions. Low threshold voltage n-MOS transistors of each of a first and a third inverter are connected to ground by a high threshold voltage n-MOS transistor. Low threshold voltage p-MOS transistors of each of a second and a fourth inverter connected to ground by a high threshold voltage p-MOS transistor. When an input logic signal is fixed at a low level during a standby state, the high threshold voltage n-MOS transistor is set to an off-state in response to a

chip select signal controlling the standby state and the high threshold voltage p-MOS transistor is set to an off-state in response to the chip select signal that is negated.

Claim 16, as amended herein, recites a method for delaying a logic signal having two logic levels consisting of a low level and a high level. A metal-oxide-semiconductor capacitor disposed on a transmission path of a logic signal is set to an off-state in an initial stage. The metal-oxide-semiconductor capacitor is changed to an on-state from the off-state according to a logic level of the logic signal. The metal-oxide-semiconductor capacitor is represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage. Claim 17 depends from Claim 16.

Claim 18, as amended herein, recites a delay circuit comprising a plurality of cascading gate circuits and a plurality of MOS capacitors connected to the output sections of the gate circuits. All the MOS capacitors are connected so as to turn from the off-state to the on-state when the logic signal having the logic level targeted for delay is input into the head gate circuit among said cascading gate circuits. Each of the MOS capacitors is represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage.

Tanaka discloses supplying a first chip enable signal for determining the operation timing of a memory chip to a first chip enable input circuit. Tanaka's Figure 7 discloses a first chip enable input circuit 1 that includes CMOS inverters 31-39, MOS capacitors 40-42 and CMOS NAND gate 43. Signal CE1 is supplied to one input terminal of the NAND gate 43 via inverters 31 to 33 The output of inverter 33 is supplied to the other input terminal of the NAND gate 43 via delay circuit 30 formed of inverters 34 and 36 and capacitors 40 to 42. The output of NAND

gate 43 is supplied to a second chip enable circuit 2 via inverters 37 to 39. (Col. 3, Line 60-Col. 2, Line 3; Figure 7).

Applicant's Claim 1, as amended herein, is neither disclosed nor suggested by the Tanaka, in that Tanaka neither discloses nor suggests ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain, said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage***, as set forth in Applicant's amended Claim 1. As described above, Tanaka discloses a delay circuit formed of inverters and capacitors in Tanaka's Figure 7. However, Tanaka appears silent on disclosing an arrangement in which the MOS capacitor is represented by a transistor having a gate fixed at one of a ground potential or source voltage. Accordingly, the reference neither discloses nor suggests the feature of ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain, said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage***, as set forth in Applicant's amended Claim 1.

For reasons similar to those set forth regarding Claim 1, Applicant's amended Claim 2 is also neither disclosed nor suggested by Tanaka. In particular, Applicant's Claim 2, as amended herein, is neither disclosed nor suggested by the reference, in that reference neither discloses nor suggests ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises: an inverter chain containing not less than one inverter; and***

***a metal-oxide-semiconductor capacitor, known as a MOS capacitor, wherein each stage is tied alternately to one of a power voltage source and a ground voltage source, said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage***, as set forth in Applicant's amended Claim 2.

For reasons similar to those set forth regarding Applicant's Claim 1, Applicant's amended Claim 16 is also neither disclosed nor suggested by Tanaka. In particular, Applicant's Claim 16, as amended herein, is neither disclosed nor suggested by the reference, in that reference neither discloses nor suggests ***a method for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising the steps of: (a) setting a metal-oxide-semiconductor capacitor disposed on a transmission path of a logic signal to an off-state in an initial stage; and (b) changing the metal-oxide-semiconductor capacitor to an on-state from the off-state according to a logic level of the logic signal, said metal-oxide-semiconductor capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage,*** as set forth in Applicant's amended Claim 16.

For reasons similar to those set forth regarding Claim 1, Applicant's amended Claim 18 is also neither disclosed nor suggested by Tanaka. In particular, Applicant's Claim 18, as amended herein, is neither disclosed nor suggested by the reference, in that reference neither discloses nor suggests ***a delay circuit comprising a plurality of cascading gate circuits and a plurality of MOS capacitors connected to the output sections of said gate circuits, wherein: all the MOS capacitors are connected so as to turn from the off-state to the on-state when the logic signal having the logic level targeted for delay is input into the head gate circuit among said cascading gate circuits, each of said MOS capacitors represented by at least one transistor***

***whose gate is fixed at one of a ground potential and a source voltage,*** as set forth in Applicant's amended Claim 18.

Applicant's Claim 15, as amended herein, is neither disclosed nor suggested by the reference, in that reference neither discloses nor suggests ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises: an inverter chain containing not less than four inverters; a p-channel metal-oxide-semiconductor transistor and an n-channel metal-oxide-semiconductor transistor, known as MOS transistors, to comprise each of the at least four inverters, wherein a gate threshold voltage of each gate is shifted in mutually opposing directions; low threshold voltage n-MOS transistors of each of a first and a third inverter connected to ground by a high threshold voltage n-MOS transistor; and low threshold voltage p-MOS transistors of each of a second and a fourth inverter connected to ground by a high threshold voltage p-MOS transistor; wherein, when an input logic signal is fixed at a low level during a standby state, said high threshold voltage n-MOS transistor is set to an off-state in response to a chip select signal controlling said standby state, and said high threshold voltage p-MOS transistor is set to an off-state in response to said chip select signal that is negated***, as set forth in Applicant's amended Claim 15. Tanaka appears silent on disclosing any arrangement in which the low threshold voltage n-MOS transistors of each of a first and a third inverter are connected to ground by a high threshold voltage n-MOS transistor. Tanaka also appears silent on disclosing any arrangement in which low threshold voltage p-MOS transistors of each of a second and a fourth inverter are connected to ground by a high threshold voltage p-MOS transistor. Accordingly, the reference neither discloses nor suggests the feature of ***low threshold voltage n-MOS transistors of each of a first and a third inverter connected to ground by a high threshold voltage n-MOS transistor; and low threshold***

***voltage p-MOS transistors of each of a second and a fourth inverter connected to ground by a high threshold voltage p-MOS transistor; wherein, when an input logic signal is fixed at a low level during a standby state, said high threshold voltage n-MOS transistor is set to an off-state in response to a chip select signal controlling said standby state, and said high threshold voltage p-MOS transistor is set to an off-state in response to said chip select signal that is negated***, as set forth in Applicant's amended Claim 15.

The Office Action states at page 2 that Tanaka's Figure 7 discloses a delay circuit. The cited reference of Tanaka includes a description corresponding to the delay circuit 30 of Figure 7 from the last line of Column 3 to the first line of Column 4 which states only that the delay circuit 30 is formed of inverters 34 to 36 and capacitors 40 to 42. Tanaka makes no mention of the targeted logic level and the delay mechanism for each logic level. Additionally, Tanaka's capacitors 40-42 appear to all be of the same type of transistor, such as an n-MOS transistor, which also differs from Applicant's claimed invention.

In view of the foregoing, Applicant respectfully submits that Claims 1-5, 9-11, and 15-17 are patentable over the reference. Accordingly, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

The rejection of Claims 5, 11, and 15 under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Hattori (U.S. Patent No. 5,459,424) is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submit that Claims 5, 11, and 15, as amended herein, are patentable over the references, taken separately or in combination.

Applicant's Claim 5 depends from independent Claim 1, and Applicant's Claim 11 depends from independent Claim 2. For reasons set forth above, Applicant's Claims 1 and 2, and claims that depend therefrom, are patentable over Tanaka. For reasons set forth below, Applicant respectfully submits that combining Tanaka with Hattori also neither discloses nor suggests Applicant's Claims 1 and 2, and claims that depend therefrom.

Applicant's independent Claims 1, 2 and 15 are summarized above.

Hattori discloses a CMOS pulse delay circuit that can accurately delay a signal by a predetermined amount. Hattori discloses inverters that each have additional switching transistors on each end, and a voltage controlled variable resistor. The indicated portion of the reference discloses a CMOS inverter that has both an N channel and a P channel transistor located after each stage of the inverter chain. (See Figure 1; Col. 1, Lines 20-60).

Applicant's Claim 1, as amended herein, is neither disclosed nor suggested by the references, taken separately or in combination, in that the references neither disclose nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain, said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage,*** as set forth in Applicant's amended Claim 1. Hattori discloses an inverter that includes an n-type MOS transistor and a p-type MOS transistor. However, Hattori is silent on disclosing a transistor included in an inverter having a gate fixed at one of a ground potential and a source voltage.

Accordingly, the references neither disclose nor suggest the feature of ***said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage***, as set forth in Applicant's amended Claim 1.

For reasons similar to those set forth regarding Claim 1, Applicant's amended Claim 2 is also neither disclosed nor suggested by the references. In particular, Applicant's Claim 2, as amended herein, is neither disclosed nor suggested by the references, taken separately or in combination, in that the references neither disclose nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises: an inverter chain containing not less than one inverter; and a metal-oxide-semiconductor capacitor, known as a MOS capacitor, wherein each stage is tied alternately to one of a power voltage source and a ground voltage source, said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage***, as set forth in Applicant's amended Claim 2.

Applicant's Claim 15, as amended herein, is neither disclosed nor suggested by the references, taken separately or in combination, in that the references neither disclose nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising low threshold voltage n-MOS transistors of each of a first and a third inverter connected to ground by a high threshold voltage n-MOS transistor; and low threshold voltage p-MOS transistors of each of a second and a fourth inverter connected to ground by a high threshold voltage p-MOS transistor; wherein, when an input logic signal is fixed at a low level during a standby state, said high threshold voltage n-MOS transistor is set to an off-state in response to a chip select signal controlling said standby state, and said high threshold***

***voltage p-MOS transistor is set to an off-state in response to said chip select signal that is negated***, as set forth in Applicant's amended Claim 15. Both Tanaka and Hattori appear silent on disclosing any arrangement in which low threshold voltage p-MOS transistors of each of a second and a fourth inverter are connected to ground by a high threshold voltage p-MOS transistor. Accordingly, the references neither discloses nor suggests the feature of ***low threshold voltage n-MOS transistors of each of a first and a third inverter connected to ground by a high threshold voltage n-MOS transistor; and low threshold voltage p-MOS transistors of each of a second and a fourth inverter connected to ground by a high threshold voltage p-MOS transistor; wherein, when an input logic signal is fixed at a low level during a standby state, said high threshold voltage n-MOS transistor is set to an off-state in response to a chip select signal controlling said standby state, and said high threshold voltage p-MOS transistor is set to an off-state in response to said chip select signal that is negated***, as set forth in Applicant's amended Claim 15.

Regarding Claim 15, the Office Action states on page 4 that Tanaka does not disclose that the inverters (34-36) are comprised of an n-MOS and a p-MOS transistor. The Office Action further states that Hattori discloses in Figure 1 that a p-channel metal-oxide-semiconductor transistor 23 and an n-channel metal-oxide-semiconductor transistor 24 comprise the inverter wherein a gate threshold voltage of each gate is shifted in mutually opposing directions. Applicant respectfully submits that the recited feature of a gate threshold voltage of each gate shifted in mutually opposing directions, as set forth in Applicant's Claim 15 and as described in the specification, for example, at page 30, lines 5-9, is neither disclosed nor suggested by Hattori.

In view of the foregoing, Applicant respectfully submits that Claims 5, 11, and 15 are patentable over the references. Accordingly, Applicant respectfully requests that the rejection be reconsidered and withdrawn.

The rejection of Claims 6 and 12 under 35 U.S.C. 103(a) as being unpatentable over Tanaka in view of Porter et al. (U.S. Patent No. 6,040,713, hereinafter referred to as "Porter") is hereby traversed and reconsideration thereof is respectfully requested. Applicant respectfully submits that Claims 6 and 12, as amended herein, are patentable over the references, taken separately or in combination.

Applicant's Claim 6 depends from independent Claim 1, and Applicant's Claim 12 depends from independent Claim 2. For reasons set forth above, Applicant respectfully submits that Claims 1 and 2, and Claims that depend therefrom, are patentable over Tanaka. For reasons set forth below, Applicant further submits that combining Tanaka with Porter also neither discloses nor suggests Applicant's Claims 1 and 2, and claims that depend therefrom.

Tanaka is summarized above.

Porter is used in the Office Action to show that a MOS capacitor represented by a p-MOS transistor is known. Applicant respectfully submits that Porter does not address the deficiencies of Tanaka as discussed above with respect to independent Claim 1. Accordingly, the references, taken separately or in combination, neither disclose nor suggest Applicant's amended Claim 1.

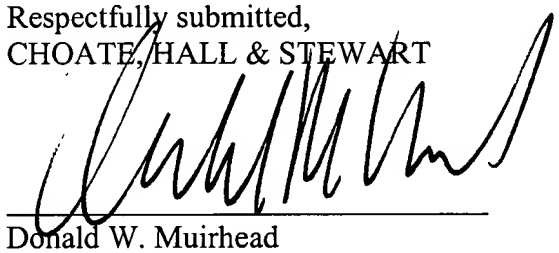
In particular, Applicant's Claim 1, as amended herein, is neither disclosed nor suggested by the references, taken separately or in combination, in that the references neither disclose nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprising: a metal-oxide-semiconductor capacitor, known as a MOS capacitor, having a single transistor per stage of the inverter chain, said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage***, as set forth in Applicant's amended Claim 1.

For reasons similar to those set forth regarding Applicant's Claim 1, Applicant's amended Claim 2 is also neither disclosed nor suggested by the references, taken separately or in combination. In particular, Applicant's Claim 2, as amended herein, is neither disclosed nor suggested by the references, taken separately or in combination, in that the references neither disclose nor suggest ***a delay circuit for delaying a logic signal having two logic levels consisting of a low level and a high level, comprises: an inverter chain containing not less than one inverter; and a metal-oxide-semiconductor capacitor, known as a MOS capacitor, wherein each stage is tied alternately to one of a power voltage source and a ground voltage source, said MOS capacitor represented by at least one transistor whose gate is fixed at one of a ground potential and a source voltage***, as set forth in Applicant's amended Claim 2.

In view of the foregoing, Applicant respectfully submits that Claims 6 and 12 are patentable over the references. Accordingly, Applicant requests that the rejection be reconsidered and withdrawn.

Based on the above, Applicant respectfully requests that the Examiner reconsider and withdraw all outstanding rejections and objections. Favorable consideration and allowance are earnestly solicited. Should there be any questions after reviewing this paper, the Examiner is invited to contact the undersigned at 617-248-4038.

Respectfully submitted,
CHOATE, HALL & STEWART



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